Pawan Kumar Fangaria

PROFESSIONAL SYNOPSIS

Pawan is a professional with high dedication and commitment in semiconductor industry. With about 25 years of working in EDA and semiconductor domain, he is yet more passionate about learning new skills and technology. This is reflected from his technical writings on new tools, technologies and designs in social media site, www.semiwiki.com.

Previously, he headed Virtuoso Physical Design Group at Cadence Noida site and before that managed semiconductor library development group at Duet Technologies (which later merged with Freescale) and developed several EDA tools at ITI Ltd., Banaglore. Thus he acquired wide technical skills in EDA, software engineering and IC design as well as management skills in various roles including project management, people management, organizational development, strategic planning, customer management and business development.

Key accomplishments in previous organizations

- **Leadership in Innovation** – Filed 5 patents
- **Successful Customer Engagement** – Significantly improved productivity of customers' IC design flows through long term collaboration. Won customers against competition by active engagement and live support to customers.
- **Quality** – Received organization level awards for improvement in tools and significant reduction in defects.
- **Organization development** – Developed Architects and Managers in the team through sustained coaching and grooming. Initiated and contributed in several organizational development initiatives, e.g. Mentorship Program at Cadence India.
- **Publications** – Wrote several blogs on EDA, Semiconductor, IC design challenges and their market dynamics. Technical paper in Cadence internal conferences (CTC, TECCI). Reviewer for CTC, TECCI, Cadence Quality Forum and VLSI93 conference.
- **Awards** – Received several organizational awards for **Excellence in Execution**, **Teaming**, **Value Practice, Quality** and **Outstanding Achievement.**

ORGANIZATIONAL EXPERIENCE

Aug'97 – Apr'11 with Cadence Design Systems, Noida, last position as Engineering Director

Work Area

- Complete Physical Design group management at Noida. New product development, deployment and support. Leading customer and business engagement. Maintenance of existing products and market share.
- EDA software tool development for Physical Design - Automatic Floorplanning, Placement and Routing, Abstract generation, Physical infrastructure and interfaces.

May'95 – Aug'97 with Duet Technology, Noida, last position as Engineering Manager

Work Area

- Electronic Design Library Development and Customer Services
- Development, delivery and services of simulation, timing and test libraries for key semiconductor companies, e.g. AMD, Vitesse, Atmel, SMOS, LSI, IKOS etc.
- In-house development of software tools and utilities for library development.

Aug'90 – May'95 with ITI Ltd., Bangalore, last position as Senior Executive Engineer

Work Area

- Development of multiple software tools for the Vinyas Standard Cell based and Full Custom design based platforms for chip design. All phases of the tool development including specification, design, code implementation, testing and integration into the main system. The tools include automatic memory generators, floorplanning for standard cells, power/ground routing, layout editor and VHDL analyzer.

QUALIFICATIONS

- Master of Engineering in Electrical Communication with 1st class from Indian Institute of Science (Bangalore) in 1990. Specialization in CAD - VLSI design.
- MBA (on-line course) with specialization in Strategy Management from The Strategy Academy, Calcutta